AMENDMENTS TO THE SPECIFICATION

IN THE TITLE

Please change to the title to read:

--EXECUTION CONTROL APPARATUS OF DATA DRIVEN INFORMATION PROCESSOR FOR INSTRUCTION INPUTS--

IN THE ABSTRACT

Please replace the Abstract of Disclosure with the following Abstract:

An execution control apparatus of a data driven information processor includes: an instruction decoder that outputs ~~the~~ a number of inputs of an instruction; a waiting data storage region that stores N (N ≥2) waiting data and respective data valid flags in one address; a constant storage that stores constants and a constant valid flag; a constant readout unit that reads out a constant and a constant valid flag from the constant storage with the node number of ~~the~~ an input packet as the address; a unit that calculates ~~the~~ a hash address and selects a process for data waiting depending upon a combination of a data valid flag, a constant valid flag, and the number of instruction inputs; and a unit that performs ~~the~~ a waiting process in response to ~~the~~ a select signal.

IN THE SPECIFICATION

On page 13, line 7, please replace the paragraph, with the following amended paragraph:

Waiting storage unit 200 further includes: a waiting region 96 ~~that~~ for storing a counterpart packet, that includes a first waiting region 96A and a second waiting region 96B forming respective partial regions; a hash calculation block 92 that calculates the hash address from the node number and generation number in input packet 89, and referring to PRE 1 and PRE 0 which are flags indicating whether first waiting region 96A/second waiting region 96B are valid or invalid, respectively by a relevant address, and determines an update value thereof according to a Table 2 that will be describe afterwards.

On page 13, line 30, and continuing to page 14, line 11, please replace the paragraph with the following amended paragraph:

The structure of waiting region 96 is shown in Fig. 15. Referring to Fig. 15, waiting region 96 includes, for each address, a PRE 0 (69) of one bit which is the data valid/invalid flag of the first waiting region and a PRE 1 (70) of one bit which is the valid/invalid flag of the second waiting region, a hash overflow address 71, an L/R 72 which is the flag to identify whether the data in the first waiting region is left or right input, seventh data 73 to 0th data 80 corresponding to the first waiting region, and seventh data 81 to 0th data ~~82~~ 88 corresponding to the second waiting region. Waiting

region 96 has the data structure of Fig. 15 for each address. More specifically, waiting region 96 includes, for each address, a region (PRE storage unit 202) storing two waiting data, and data valid flag PRE 1/0 of each waiting data. PRE storage unit 202 includes two D flip-flop circuits to store corresponding data valid flag PRE 1/0 for each address in the apparatus of the present embodiment. These D flip-flop circuits include a reset terminal and are cleared in response to a reset signal RESET.